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EXAMINER	
MAI, A	
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2814	

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MM92/0411

DATE MAILED: 04/11/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/392,034	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

1. Claims 1 and 6 are rejected under 35 U.S.C. 102(e) for being clearly anticipated by Omid-Zohoor (U.S. Patent No. 6,097,072) as previously applied.

2. Claims 7, 8 and 11 are rejected under 35 U.S.C. 102(e) for being clearly anticipated by Omid-Zohoor '072 as previously applied.

3. Claims 2-5 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 as applied to claim 1 above and further in view of Poon et al. (U.S. Patent No. 5,387,540) as previously applied.

4. Claims 9, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 as applied to claim 7 above, and further in view of Lee '316 as previously applied.

5. Claims 18-22 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 in view of Lee '316 as previously applied.

6. Claim 23 is rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 and Lee '316 as applied to claim 18 above, and further in view of Poon '540 as previously applied.

7. Claim 24 is rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 in view of Lee '316 as previously applied.

8. Claim 25 is rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 in view of Lee '316 as previously applied.

9. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 in view of Lee '316 as previously applied.

10. Claims 28-30 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 in view of Lee '316 as previously applied.

11. Insofar as understood by examiner, claims 35-37 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 in view of Lee '316 as previously applied.

12. Insofar as understood by examiner, Claim 38 is rejected under 35 U.S.C. 102(e) for being clearly anticipated by Omid-Zohoor '072 as previously applied.

13. Insofar as understood by examiner, claims 39 and 40 are rejected under 35 U.S.C. 103(a) for being unpatentable over Omid-Zohoor '072 as applied to claim 38 above, and further in view of Lee '316 as previously applied.

14. Insofar as understood by examiner, Claim 41 is rejected under 35 U.S.C. 102(e) for being clearly anticipated by Omid-Zohoor '072 as previously applied.

Terminal Disclaimer

15. The terminal disclaimer filed on January 29, 2001 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 5,953,621 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

16. Claims 35-37, 38-40 and 41 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

A new limitation of these claims includes: "wherein said spacer and said isolation trench are ***formed*** with a single etch recipe".

The specification describe a process including: "the spacer etch and the isolation trench etch can be carried out with a single etch recipe that is ***selective to*** insulation film 26". (Fig. 4A-B, page 11, lines 13-14). The term "***selective to***" is well known and recognized in the art to be acted on one material, in this case silicon substrate 12, selective to the background material, in this case film 26. The term "single etch recipe" means one kind of etchant. An etchant that "***selective to***" insulation film 26 means it does not remove insulation film 26.

How can an etchant *selective to* the insulation film 26 remove the silicon substrate 12 to form trenches 32 when the substrate is still covered by film 26?

If a single etch recipe that is *selective to* film 26 also etch film 26 to form the spacer 28 then what happen to the island 22 of a different material?

It appears that the trench is much more deeper than the thickness of the film 26.

How can trench 32 is formed in a single etch and the spacer 28 still remained?

As best understood by examiner, the formation of the spacers 28 and trench 32 requires two etch steps. One etch step selective to island 22 to form spacers 28 and the second etch step selective to spacers 28 and island 22 to form trenches 32.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

17. Claim 43 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor (U.S. Patent No. 6,097,072).

Omid-Zohoor teaches a method of forming a microelectronic structure as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) upon the oxide layer;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (360) extending below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344), the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures; and

planarizing the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures to form a planar upper surface from the conformal

second layer and the first and second spacers (356) of the respective first and second isolation structures, and being situated above the oxide layer wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches. (See Figs. 3A-M).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Poon et al. (U.S. Patent No. 5,387,540).

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) upon the oxide layer;

selectively removing the silicon nitride layer to exposed the oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) over the oxide layer and the silicon nitride layer;

selectively removing the first silicon dioxide layer to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each spacer is situated upon the oxide layer, is in contact with the silicon nitride layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

forming a corresponding electronically active region below the termination of each isolation trench within the semiconductor substrate;

filling each isolation trench with a conformal second silicon dioxide layer (364), the conformal second silicon dioxide layer within each isolation trench extending above the oxide layer in contact with a corresponding pair of the spacers; and

selectively removing the conformal second silicon dioxide layer and the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and being situated above the pad oxide layer, wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor teaches all of the features of the claim with the exception of forming a liner upon a sidewall of each isolation trench.

However, Poon teaches forming a trench liner (28) upon a sidewall of each isolation trench, the liner extending from an interface thereof with the oxide layer (14) to the termination of the isolation trench within the semiconductor substrate (12). (See Fig. 4).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the liner (28) upon a sidewall of each isolation trench (360) of Omid-Zohoor as taught by Poon to release stress on the trench surface.

With respect to claim 15, the liner (28) of Poon is thermally grown oxide of the semiconductor substrate.

With respect to claim 16, the liner (50) of Poon is composed of silicon nitride. (see Fig. 11).

With respect to claim 17, the method of Omid-Zohoor further includes:

removing the pad oxide layer upon portion of the surface of the semiconductor substrate; and

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate.

19. Claims 31, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee et al. (U.S. Patent No. 5,229,316).

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming a pad oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) over semiconductor substrate;

selectively removing the silicon nitride layer to expose the oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) conformally over the oxide layer and the silicon nitride layer;

selectively removing the first silicon dioxide layer to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each the spacer is upon the pad oxide layer, is in contact with the silicon nitride layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the pad oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal second layer (364), the second layer extending above the oxide layer in contact with a corresponding pair of the spacers; and

planarizing the conformal second layer and each spacer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces and is situated above the pad oxide layer;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340), the doped region below each isolation trench and forming a liner on the sidewall of the trench.

However, Lee teaches forming a polysilicon layer (36) between the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed form the oxide layer and the first dielectric layer.

Lee, further, teaches forming a corresponding doped region (26) below the termination trench within the semiconductor substrate (12). (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region (26) below the termination of each isolation trench (360) within the semiconductor substrate (120) of Omid-Zohoor as taught by Lee to provide further electrical isolation effect between circuit components.

Additionally, Lee teaches forming a liner (24) upon the sidewall of each isolation trench, extending from an interface thereof with the pad oxide layer (14) to the termination of the isolation trench (22) within the semiconductor substrate (12). (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the liner (24) upon the sidewall of each isolation trench prior to filling each isolation trench (360) of Omid-Zohoor as taught by Lee to release stress on the trench surface.

With respect to claim 32, as best understood by examiner, the liner (24) of Lee is thermally grown oxide of the semiconductor substrate, and wherein the conformal second layer (364) of '072 is composed of an electrically insulative material.

With respect to claim 34, the method of Omid-Zohoor further includes:

exposing the pad oxide layer (340) upon a portion of a surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the semiconductor substrate; and

forming a layer (384) composed of polysilicon upon the gate oxide layer (380) in contact with a pair of the spacers; and

selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surface. (See Fig. 3Q).

20. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 and Lee '316 as applied to claim 31 above, and further in view of Poon '540.

Omid-Zohoor '072 and Lee '316 are shown to teach all of the features of the claim with the exception of forming liner (24) composed of silicon nitride.

However, Poon teaches forming liner (50) comprises silicon nitride upon the isolation trench (22).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form liner (24) of Omid-Zohoor, in view of Lee '316, comprises silicon nitride (50) as taught by Poon '540 to protect the substrate from further oxidizing.

21. Claim 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) over the semiconductor substrate;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (360) extending below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer, the second spacer of the second isolation

structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (364), composed of an electrically insulative material, filling the first and second isolation trenches and extending continuously therebetween and above the oxide layer in contact with the first and second spacers of the respective first and second isolation structures; and

forming a planar upper surface from the conformal second layer and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in hart by the active area, the second layer and the first and second isolation trenches. (See Figs. 3A-M, col. 4, l. 1-col. 5, l. 4).

Thus, Omid-Zohoor teaches all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340).

However, Lee teaches forming a polysilicon layer (36) between the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed form the oxide layer and the first dielectric layer.

Response to Arguments

22. Applicant's arguments filed January 29, 2001 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

Regarding claims 1 and 7, applicant recognizes that the trenches 360 of Omid-Zohoor '072 are filled with oxide layer 364 or with an insulating material that conforms to the trenches and to the surface of the rest of the wafer. See Amendment "B" and Response page 19. Applicant argues about the process steps of Omid-Zohoor '072 between the deposition and planarizing of the conformal oxide layer 364. Insofar as the claim limitation is concerned, Omid-Zohoor '072 teaches each and every elements of the claims including: "planarizing the *conformal* layer (364)... to form thereform an upper surface for each said isolation trench that is co-planar to the other said upper surfaces" (italicization added). The limitation of the claims fails not preclude one or more steps between the filling and planarizing the *conformal* layer (364).

The rejection of claims 1 and 7 and the dependent claims thereof for being clearly anticipated by Omid-Zohoor '072, is therefore, maintained.

Claim Rejections - 35 USC § 103(a)

Applicant's argument appears to rely on the previously discussed subject matter of the rejection under *35 USC § 102*. These features concern the formation of a conformal layer 364 and the subsequent planarization of this conformal layer (claims 2-5, 9-10, 12-13, 14-34 and 42).

As previously discussed, applicant has recognized the deposition of the conformal layer 364 and argues about the intervening steps before the planarization. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *no other steps between the deposition and the planarization of the conformal layer*) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding the new limitation of "wherein said spacers and said isolation trenches are formed with a single etch recipe".

Insofar as the specification is concerned, the single etch to form both spacers 28 and trenches 32 was not described in the specification in such a way as to enable one skilled in the art to carry out using a single etch recipe that is selective to insulation film 26, while the insulation film 26 still covering the substrate.

If an etchant that selective to insulation film 26, said etchant can not remove insulation film 26, thus trenches 32 does not exist.

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
April 9, 2001

OLIK CHAUDHURI
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